Hi3718C V100 Brief Data Sheet

Key Specifications

CPU

- Dual-core ARM Cortex A9 processor
- Independent I-cache, D-cache, and L2 cache
- Integrated multimedia acceleration engine NEON
- Hardware Java acceleration
- Integrated hardware floating-point coprocessor

3D GPU

- Quad-core high-performance GPU
- OpenGL ES 2.0/1.1/1.0 and OpenVG 1.1
- EGL

Memory Interfaces

- DDR3/3L SDRAM interface
  - Maximum 2 GB memory capacity
  - 32-bit wide memory
  - Maximum 800 MHz or 1600 MHz frequency
- SPI flash interface
  - 1-/2-/4-bit flash memory
  - Maximum 32 MB SPI flash capacity
- NAND flash interface
  - SLC/MLC NAND flash
  - Toggle 1.0/2.0 or ONFI 2.0/3.0
  - 8-bit data width
  - Maximum 64 GB NAND flash capacity
  - Maximum 80-bit ECC
- eMMC flash interface

Video Decoding

- H.264 BP/MP/HP@ level 5.0; MVC
- MPEG1
- MPEG2 SP@ML and MP@HL
- MPEG4 SP@L0–3 and ASP@L0–5; GMC
- MPEG4 short header format (H.263 baseline)
- AVS baseline @level 6.0 and AVS+ (AVS-P16)
- VC-1 SP@ML, MP@HL, and AP@L0-3
- VP6/VP8
- 1080p@60 fps decoding
- Low-delay decoding
- Simultaneous multi-channel decoding

Image Decoding

- Full HD JPEG hardware decoding, a maximum of 64 megapixels
- MJPEG baseline decoding, a maximum of 1080p@40 fps decoding capability
- PNG hardware decoding, a maximum of 64 megapixels

Video and Image Encoding

- H.264 BP/MP/HP@level 4.2 video encoding, a maximum of 1080p@30 fps encoding capability
- JPEG hardware encoding, a maximum of 1080p@30 fps encoding capability
- CABAC
- VBR or CBR mode for video decoding
- Inter-frame prediction and intra-frame prediction
- Fast motion estimation algorithm
- Low-delay encoding
- Encoding of multiple ROIs

Audio Encoding and Decoding

- Dedicated audio DSP
- G.711(u/a) audio decoding
- MPEG L1/L2
- DRA decoding
- Dolby Digital and Dolby Digital Plus
- Dolby True HD and Dolby Digital Plus transcoding
- DTS and DTS HD core decoding
- DTS and Dolby Digital transparent transmission
- AAC-LC and HE AAC V1/V2 decoding
- APE, FLAC, Ogg, AMR-NB, and AMR-WB decoding
- Down mixing and resampling
- 2-channel audio mixing and echo cancellation
- Intelligent volume control
- SRS, Dolby, and MS11 sound effects
- Pounding bass processing
- G.711(u/a), AMR-NB, AMR-WB, and AAC-LC encoding

Graphics and Display Processing

- Hardware overlaying of multi-channel graphics and video inputs
- 5-layer OSD
- Four video layers
- Mosaic and multi-region display
- Mirroring display
- 16-bit or 32-bit color depth
- Image or video rotation
- Letterbox and pan and scan
- 3D video processing and display
- Multi-tap vertical and horizontal scaling of videos and graphics; free scaling
- Low-delay display
- Enhanced full-hardware TDE
- Full-hardware anti-aliasing and anti-flicker
- CSC with configurable coefficients
- Image enhancement and denoising
- Deinterlacing
- Sharpening
- Chrominance, luminance, contrast, and saturation adjustment
- Db/Dr processing for graphics and videos

Audio and Video Interfaces

- PAL, NTSC, and SECAM standard output, and forcible standard conversion
- Aspect ratio of 4:3 or 16:9 and forcible aspect ratio conversion
- 1080p60/1080p50/1080p30/1080p24/1080i60/1080i50 /720p/576p/576i/480p/480i outputs
- One SD output and one HD output from the same source or

different sources

- Digital video interfaces
  - One HDMI 1.4a TX with HDCP1.2 output interface
  - One BT.656/601 or BT.1120 video input interface and extended HDMI 1.4a RX input interface
  - One BT.1120 video output interface
  - One LCD output interface
- Analog video interfaces
  - One CVBS interface
  - One embedded VDACs that integrate video buffers and support cable detection
  - Rovi and VBI
- Audio interfaces
  - Audio-left and audio-right channels
  - SPDIF interface
  - Embedded ADAC
  - Two I^2S or PCM digital audio inputs/outputs
  - HDMI audio output

Peripheral Interfaces

- One SATA 3.0 host interface
- Three USB 2.0 host ports, one supporting the host/device function
- One 4-bit SDIO 3.0 interface with integrated LDO, supporting 3.3 V or 1.8 V components
- Two 10/100/1000 Mbit/s GE MACs with one integrated Fast Ethernet PHY
- Two smart card interfaces, supporting T0, T1, and T14 protocols
- One IR receiver with two input interfaces
- One LED and keypad control interface
- Four I^2C interfaces
- Five UART interfaces
- Multiple GPIO interfaces
- Four PWM interfaces
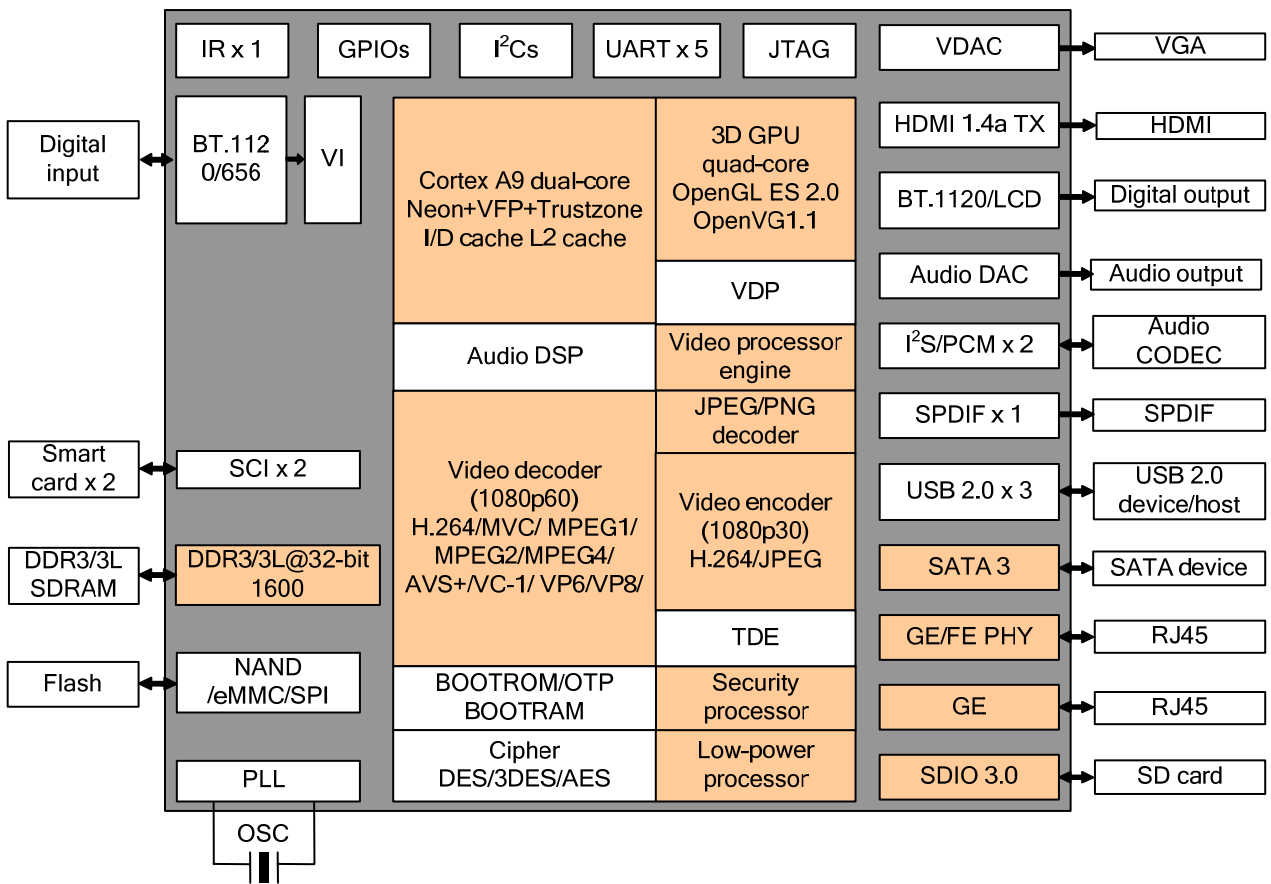- Integrated POR module

Others

- 2-layer PCB design
- Various boot modes
- Boot program download and execution over a serial port or USB port
- Integrated standby processor, supporting various low-power modes and less than 30 mW standby power consumption
- Low-power design such as AVS and DVFS
- 2.5 W typical working power consumption
- PBGA558 package with 23 mm x 23 mm (0.91 in. x 0.91 in.) body size and 0.8 mm (0.03 in.) pitch
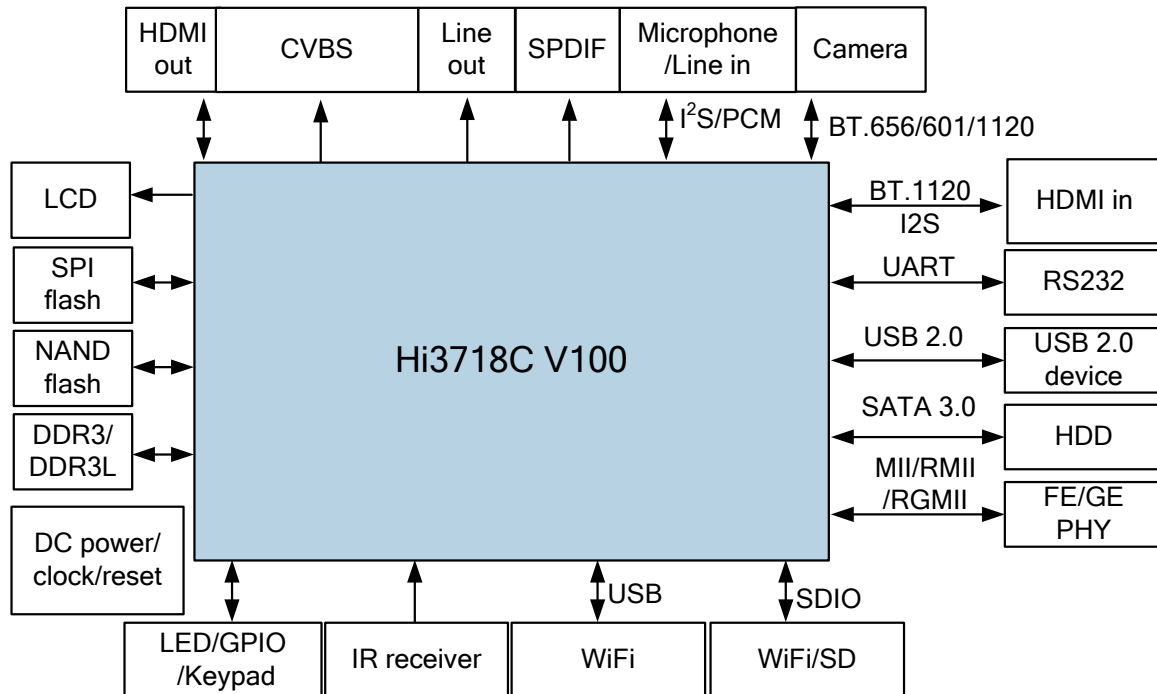
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Functional Block Diagram

With an integrated high-performance Cortex A9 dual-core processor and embedded NEON, Hi3718C V100 meets differentiated service requirements. To meet the growing requirements on multimedia playback, video communication, and multi-screen transcoding, Hi3718C V100 supports HD video decoding in various formats, including H.264, MVC, MPEG1, MPEG2, MPEG4, AVS+, VC-1, VP6, and VP8, and high-performance H.264 HD encoding. Hi3718C V100 provides a smooth man-machine interface and rich gaming experience with a high-performance 2D/3D acceleration engine. It also enables flexible connection schemes with two GE ports, three USB 2.0 ports, one SATA port, and more peripheral interfaces.

Typical Application Block Diagram

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Acronyms and Abbreviations

ADAC	audio DAC
AES	advanced encryption standard
AVS	audio/video coding standard
AVS	adaptive voltage scaling
CABAC	context-based adaptive binary arithmetic coding
CBR	constant bit rate
CSC	color space conversion
CVBS	composite video broadcast signal
DES	data encryption standard
DRM	digital rights management
DSP	digital signal processor
DVFS	dynamic voltage and frequency scaling
GPIO	general purpose input/output
GPU	graphics processing unit
HDCP	high-bandwidth digital content protection
HDMI	high definition multimedia interface
I/O	input/output
I^2C	inter-integrated circuit
I^2S	inter-IC sound
IR	infrared
LCD	liquid crystal display
MLC	multi-level cell
OTP	one-time programmable
PBGA	plastic ball grid array
PCM	pulse code modulation
PID	packet ID
POR	power-on reset
PVR	personal video recorder
PWM	pulse width modulation
ROI	region of interest
SLC	single-level cell
SPDIF	Sony/Philips digital interface
UART	universal asynchronous receiver transmitter
VBR	variable bit rate
VDAC	video digital-to-analog converter

Postal Code: 518129   5   www.hisilicon.com
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